

KASLR: Break It, Fix It, Repeat

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ACM AsiaCCS 2020

Graz University of Technology



- Meltdown requires **hardware mitigations**



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- How do these mitigations work?



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- How do these mitigations work?
- Microarchitectural KASLR breaks are **fast and reliable**



- Meltdown requires **hardware mitigations**
- How do these mitigations work?
- Microarchitectural KASLR breaks are **fast and reliable** → how do we **prevent them**?



MELTDOWN

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- Meltdown can **read** any **kernel** address



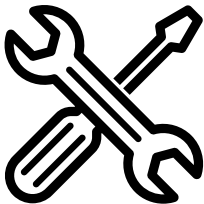
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MELTDOWN

- CPU uses data in **out-of-order execution** before permission check
 - Meltdown can **read** any **kernel** address
 - **Physical memory** is usually mapped in kernel
- Read arbitrary memory



Assumptions

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Hypothesis

Load is executed, returned value is **zeroed out**



Two tests:

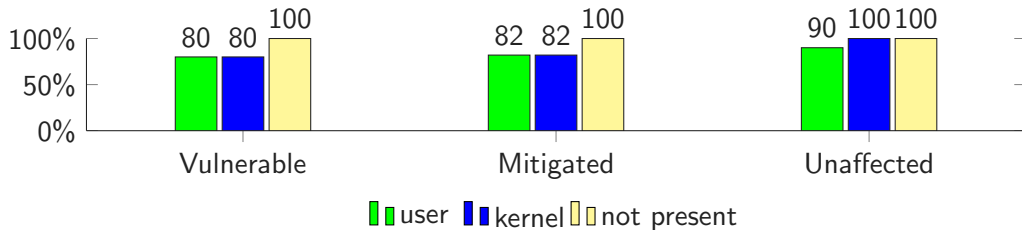
1. Perform **Meltdown attack**



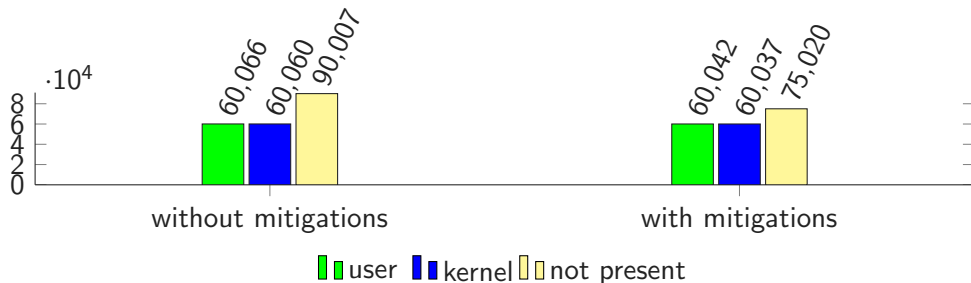
Two tests:

1. Perform Meltdown attack
2. Use Performance Counters

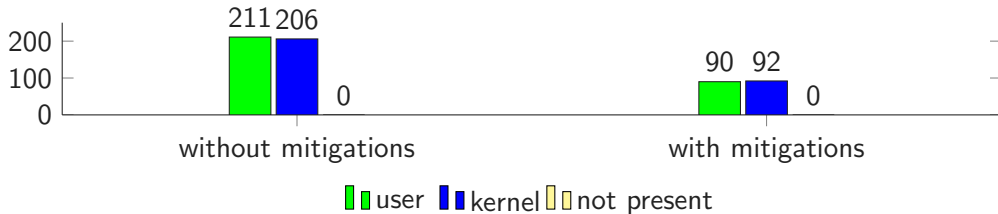
- Intel: CYCLE_ACTIVITY.STALLS_MEM_ANY
- AMD: Dispatch Stalls



- Track number of **issued μ OPs** on the load ports
- UOPS_DISPATCHED_PORT.PORT_2, UOPS_DISPATCHED_PORT.PORT_3



- L1D_PEND_MISS.PENDING_CYCLES





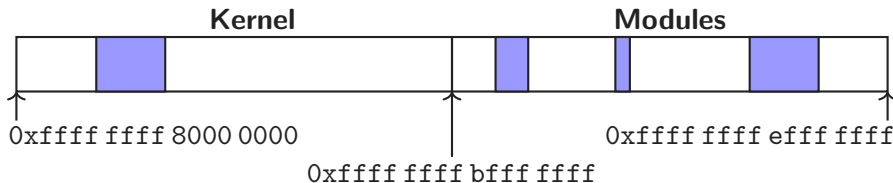
- Can we use the hardware-based mitigations for an attack?

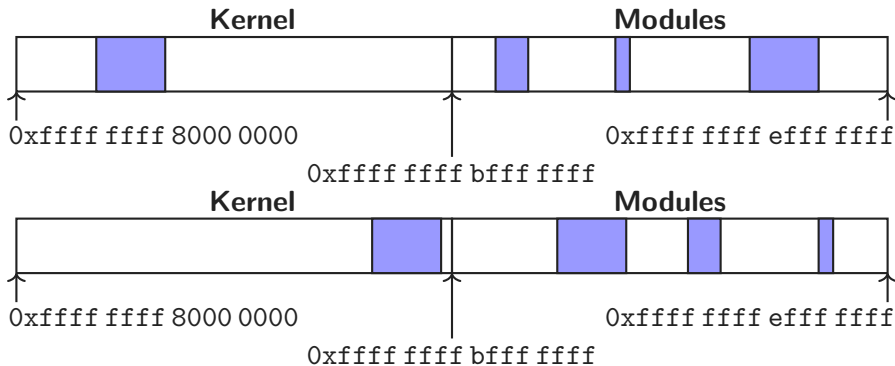


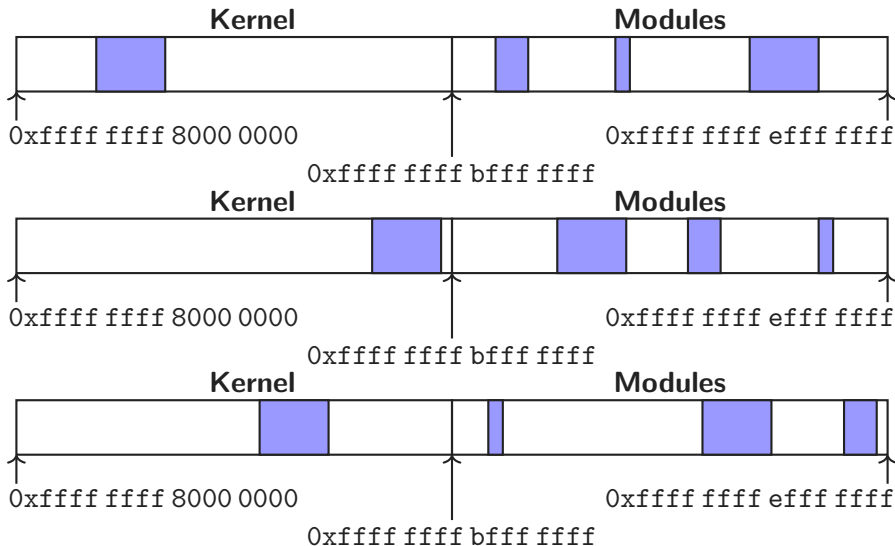
- Can we use the hardware-based mitigations for an attack?
- EchoLoad: fast and reliable **KASLR break**



- Can we use the hardware-based mitigations for an attack?
- EchoLoad: fast and reliable **KASLR break**
- **Encodes** the returned value in the **cache**

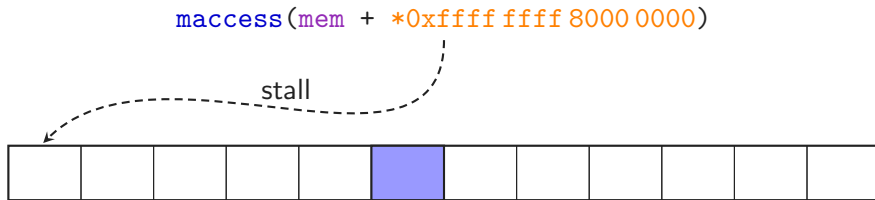


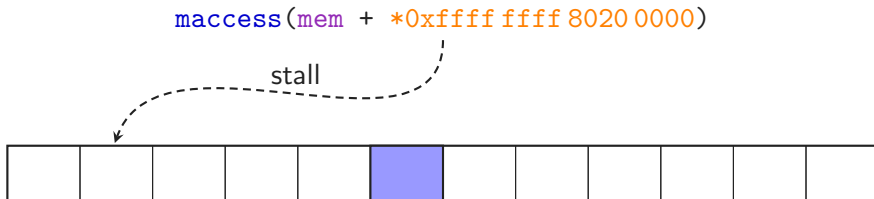




```
maccess(mem + *0xffff ffff 8000 0000)
```







```
maccess(mem + *0xffff ffff 8040 0000)
```

stall



```
maccess(mem + *0xffff ffff 8060 0000)
```

stall

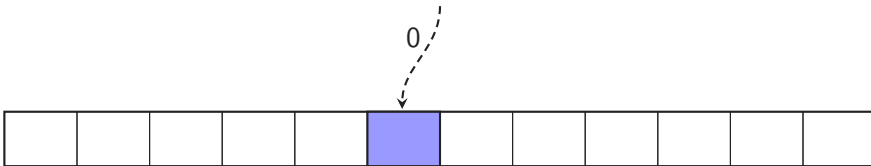


```
maccess(mem + *0xffff ffff 8080 0000)
```

stall



```
maccess(mem + *0xffff ffff 80a0 0000)
```



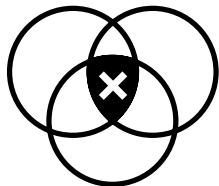
CPU		Speculation		TSX		Segfault	
i7-6700K	Time (F-Score)	63 μ s	(0.999)	48 μ s	(1.000)	133 μ s	(1.000)
i9-9900K	Time (F-Score)	33 μ s	(1.000)	29 μ s	(1.000)	86 μ s	(1.000)
Xeon Silver 4208	Time (F-Score)	51 μ s	(0.994)	40 μ s	(1.000)	127 μ s	(1.000)

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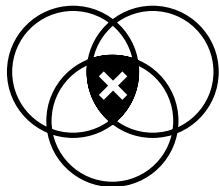
- Works in **SGX** and **JavaScript**

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- Works in **SGX** and **JavaScript**
- Enables **Meltdown from JavaScript** on unpatched x86

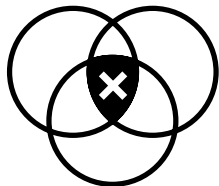


Timing difference



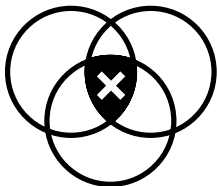
Timing difference

- between mapped and unmapped pages



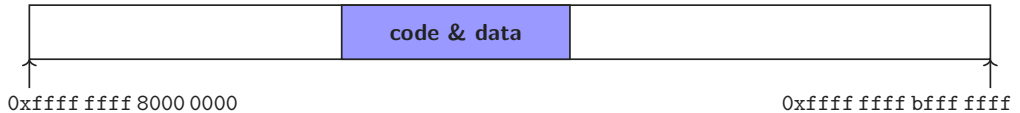
Timing difference

- between mapped and unmapped pages
- for different page sizes

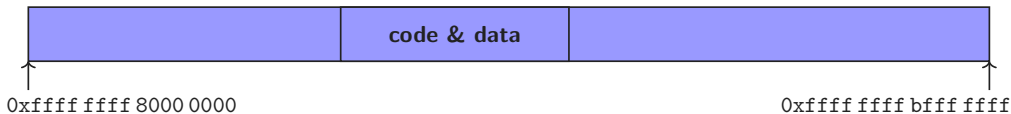


Timing difference

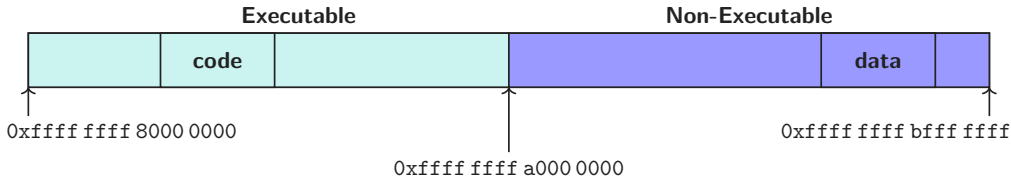
- between mapped and unmapped pages
- for different page sizes
- between executable and non-executable pages



Current Linux design



Step 1: Mitigating difference between mapped and unmapped pages

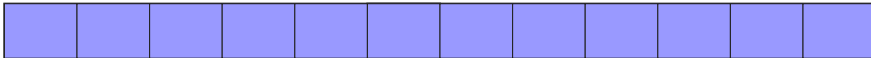


Step 2: Mitigating difference between **executable** and **non-executable** pages

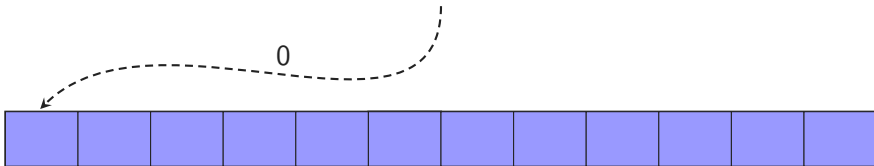
```
maccess(mem + *0xffff ffff a000 0000)
```



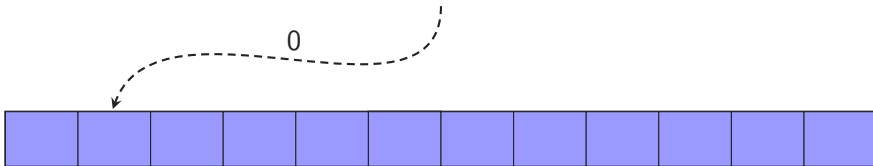
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maccess(mem + *0xffff ffff a000 0000)
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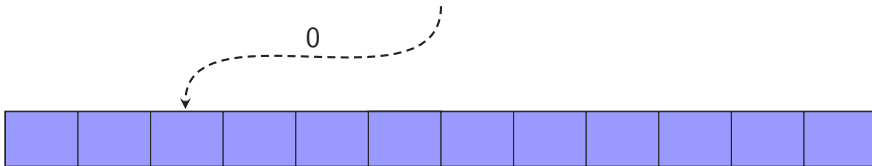
```
maccess(mem + *0xffff ffff a000 0000)
```



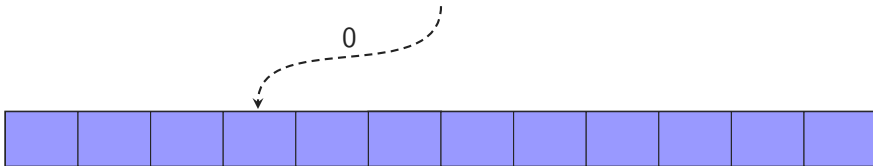
```
maccess(mem + *0xffff ffff a020 0000)
```



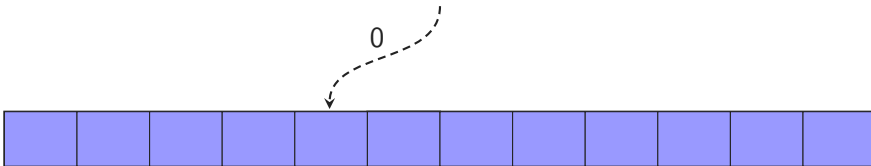
```
maccess(mem + *0xffff ffff a040 0000)
```



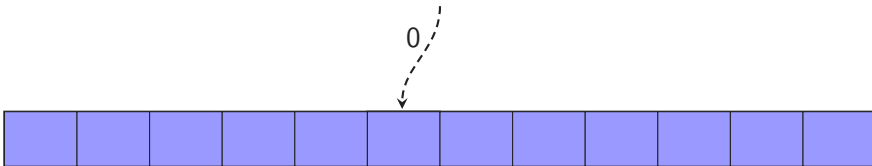
```
maccess(mem + *0xffff ffff a060 0000)
```



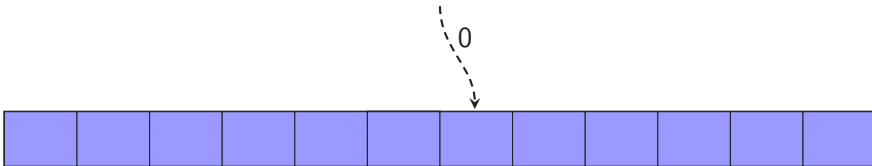
```
maccess(mem + *0xffff ffff a080 0000)
```



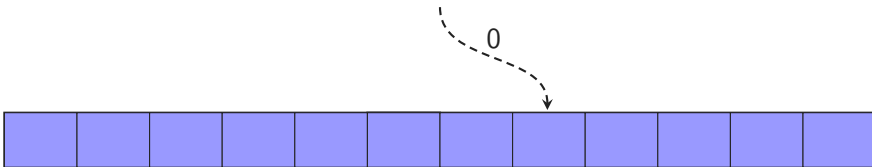
```
maccess(mem + *0xffff ffff a0a0 0000)
```



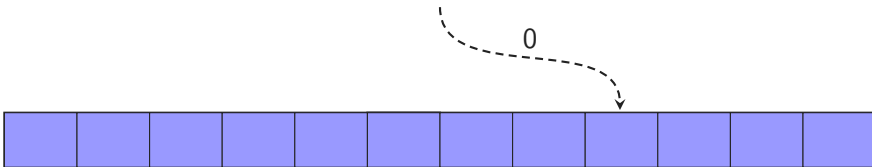
```
maccess(mem + *0xffff ffff a0c0 0000)
```



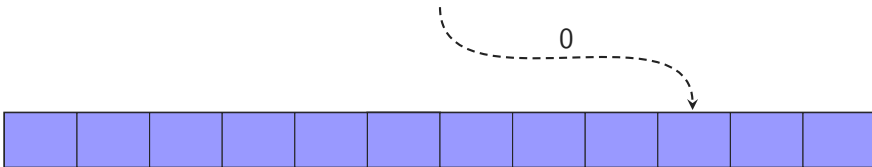
```
maccess(mem + *0xffff ffff a0e0 0000)
```



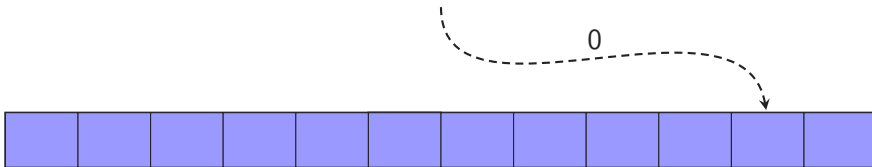
```
maccess(mem + *0xffff ffff a100 0000)
```



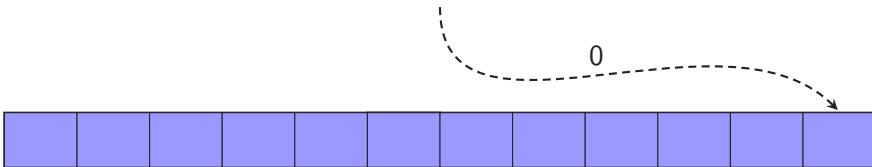
```
maccess(mem + *0xffff ffff a120 0000)
```

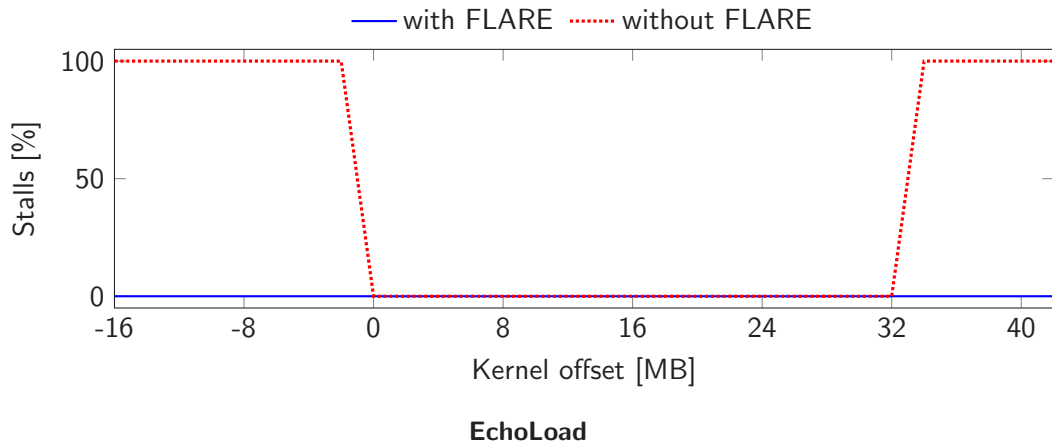


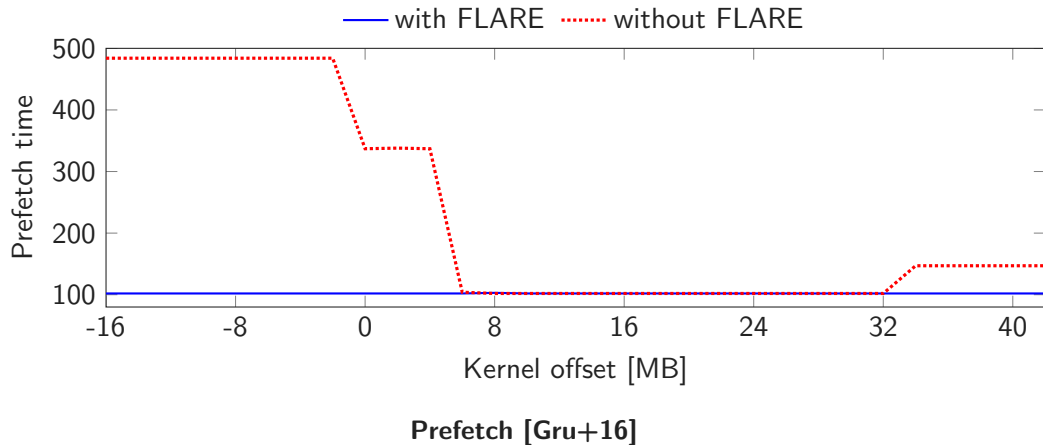
```
maccess(mem + *0xffff ffff a140 0000)
```

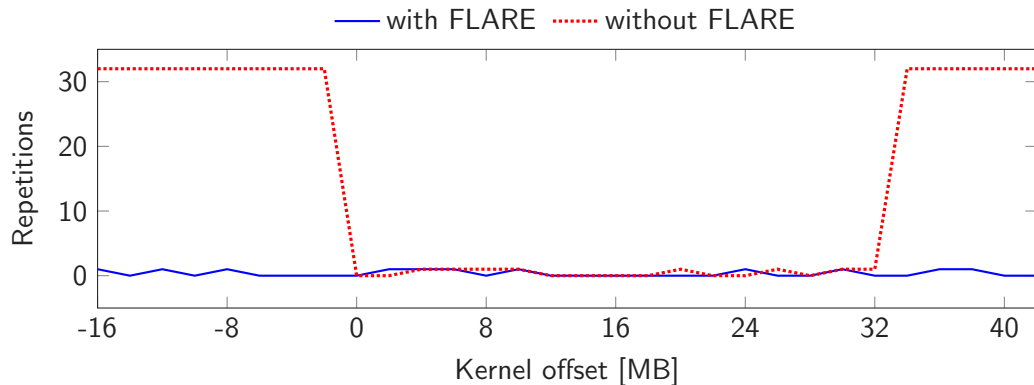


```
maccess(mem + *0xffff ffff a160 0000)
```

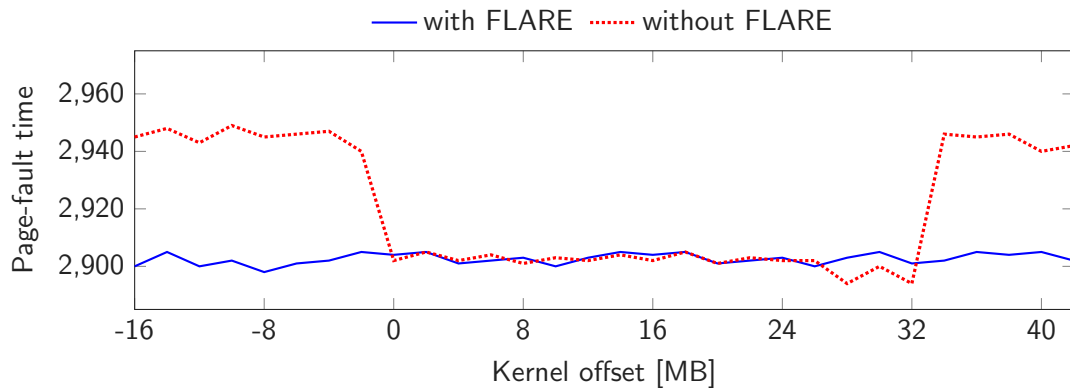




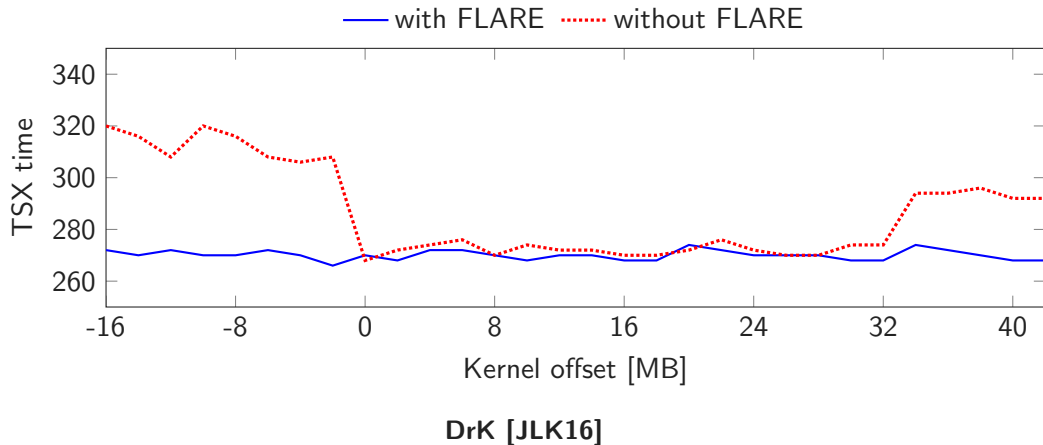


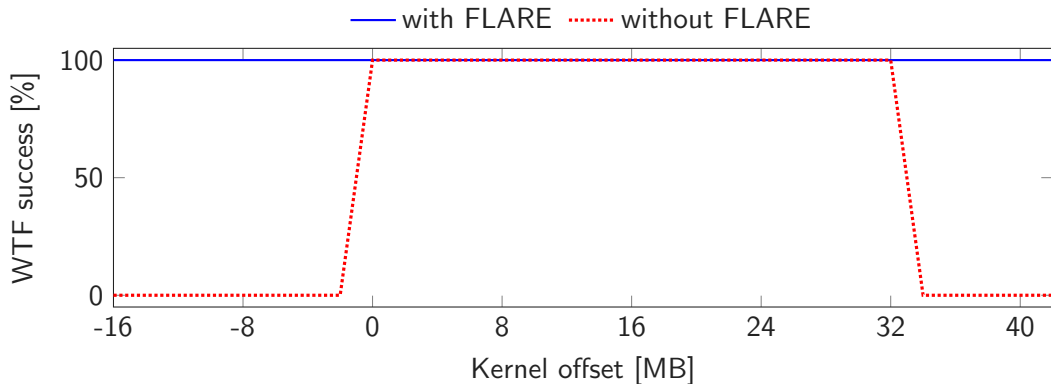


Data Bounce [Sch+19]



Double page fault [HWH13]





Fallout [Can+19]



You can find our **proof-of-concept** implementation of FLARE on:

- <https://github.com/IAIK/FLARE>



More details in the **paper** [Can+20]

- Attacks from and on SGX
- Meltdown in JavaScript
- Kernel modules, vmalloc, ...
- ...



AsiaCCS'20

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- Reverse-engineered **hardware mitigations** in recent Intel CPUs
 - Presented a new attack based on these mitigations
 - Proposed a mitigation for recent **microarchitectural KASLR breaks**
- Need to consider impact **mitigations have on security**

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References



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